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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/057,225	01/25/2002	Leonard Forbes	303.506US4	3248

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EXAMINER
TRINH, MICHAEL MANH

ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 09/03/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Offic Action Summary	Application No. 10/057,225	Applicant(s) FORBES, LEONARD	
	Examiner Michael Trinh	Art Unit 2822	

-- Th MAILING DATE of this communication appears on th cover she t with the correspond nce address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 June 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☒ The proposed drawing correction filed on *02 June 2003* is: a)☒ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a)☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

*** This office action is in response to Applicant's Amendment and RCE filed on June 02, 2003. Claims 1-30 are pending.

*** The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Claim Rejections - 35 USC § 112

1. Claims 1-13,21-30 are is rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention; and/or as based on a disclosure which is not enabling.

Re base claims 1,8,9,13, and 21: Original specification does not teach the claimed method including the recitation of the step of forming an insulating layer on the substrate at the beginning (e.g. before the other steps, such as forming a first source/drain region). For example, as shown in Figure 5C, the insulating layer 902 is formed on the substrate after forming other source, drain and body regions.

(Dependent claims are rejected as depending on rejected base claim)

Claim Rejections - 35 USC § 103

2. Claims 1-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mazure et al (5,308,782) taken with Colinge (Article of "Reduction of Kink Effect...").

Mazure teaches (at Figs 1-14; col 3, line 1 through col 8) a method for forming a transistor on a substrate comprising at least the main steps of: forming a silicon on insulator (SOI)including an insulating layer on the substrate (col 3, lines 1-10); forming a first source/drain region 28 on the substrate (col 4, lines 26-55); vertically forming a body region on the first source/drain region, wherein vertically forming the body region 30 includes vertically growing an epitaxial layer and wherein the body region includes opposing sidewall surfaces (Figs 4 and 9; col 4, line 56 through col 5, line 44); forming a second source/drain region 32/34 on the body region 30; forming a first gate 18/19 on a first one of the opposing sidewall surfaces with a first gate oxide 22 therebetween; forming a second gate 18 on a second oxide of the second one of the opposing sidewall surfaces with a second gate oxide 22 therebetween (Figs 4

and 9-10), wherein forming first source/drain region by ion implantation or epitaxial growing (col 4, lines 36-55).

Mazure lacks to form the body region as a fully depleted structure.

However, Colinge teaches to form a thin film transistor comprising a thin body channel region as fully depleted structure (page 97, left column; page 99), wherein the body region having a thickness of about 100 nm.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the transistor body region of Mazure to have a thin thickness as taught by Colinge so as to form the thin film transistor comprising a thin body channel region operated as fully depleted structure. This is because of the desirability to reduce kink effect, current overshoots, and to form a very thin transistor. Additionally, the subject matter as a whole would have been obvious to one of ordinary skill in the art at the time the invention was made to select the portion of the prior art's range of thickness, as taught by the references including Mazure and Colinge, which is within the range of applicant's claims, because it has been held to be obvious to select a value in a known range by optimization for the best results, see In re Aller, etal., 105 USPQ 233; In re Waite 77 USPQ 586 (CCPA 1948); In Re Swanson 56 USPQ 372 (CCPA 1942).

3. Claims 1-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bertin et al (6,060,746) taken with Mazure et al (5,308,782).

Bertin et al teach a method (Figs 6,7,3A-9; cols 4-6) for forming a transistor on a substrate comprising at least the main steps of: forming a first source/drain region on the substrate; vertically forming a body region 19 on the first source/drain region 23,12 (Figs 6,7) as a fully depleted structure (col 2, lines 17-21), wherein vertically forming the body region 19 includes vertically growing an epitaxial layer and wherein the body region includes opposing sidewall surfaces (Figs 6,7; col 4, line 65 through col 5); forming a second source/drain region 22 on the body region; forming a first gate 15 on a first one of the opposing sidewall surfaces with a first gate oxide 18 therebetween (col 6); forming a second gate 15 on a second oxide 18 of the second one of the opposing sidewall surfaces with a second gate oxide therebetween, wherein forming first source/drain region by ion implantation, epitaxial growing or combination thereof

(col 3, lines 40-47), wherein the body channel region having a thickness of 0.18 micron (col 2, lines 43-60), wherein the body region is encased with a ASG film and then annealing to diffuse the N-type dopant (col 5, lines 20-67), wherein CVD depositing and employing a BSG film as well known in the art for providing P-type dopant would have been obvious to one of ordinary skill in the art.

Berlin lacks forming an insulating layer on the substrate.

However, Mazure teaches (at col 3, lines 1-10) forming a transistor on a substrate, wherein the substrate includes a bulk silicon substrate or a silicon on insulator (SOI) substrate including a silicon layer on an insulating layer on a silicon substrate.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the transistor of Berlin on a silicon on insulator (SOI) substrate including an insulating layer on a silicon substrate as taught by Mazure, because these alternative substrates are art recognized alternative for substitution, wherein substrate capacitance is reduced due to the insulating layer formed on the silicon substrate.

Claim Rejections - 35 USC § 102

4. Claims 14-19 are rejected under 35 U.S.C. 102(e) as anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over Bertin et al (6,060,746).

Bertin et al teach a method (Figs 6,7,3A-9; cols 4-6) for forming a transistor on a substrate comprising at least the main steps of: forming a first source/drain region on the substrate; vertically forming a body region 19 on the first source/drain region 23,12 (Figs 6,7) as a fully depleted structure (col 2, lines 17-21), wherein vertically forming the body region 19 includes vertically growing an epitaxial layer and wherein the body region includes opposing sidewall surfaces (Figs 6,7; col 4, line 65 through col 5); forming a second source/drain region 22 on the body region; forming a first gate 15 on a first one of the opposing sidewall surfaces with a first gate oxide 18 therebetween (col 6); forming a second gate 15 on a second oxide 18 of the second one of the opposing sidewall surfaces with a second gate oxide therebetween, wherein forming first source/drain region by ion implantation, epitaxial growing or combination thereof (col 3, lines 40-47), wherein the body channel region having a thickness of 0.18 micron (col 2, lines 43-60), wherein the body region is encased with a ASG film and then annealing to diffuse

the N-type dopant (col 5, lines 20-67), wherein CVD depositing and employing a BSG film as well known in the art for providing P-type dopant would have been obvious to one of ordinary skill in the art.

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

5. Claims 1-30 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-22 of U.S. Patent No. 6,320,222 taken with Mazure (5,308,782).

Although the conflicting claims are not identical, they are not patentably distinct from each other because Patent claims also include and recite a method for forming the dual-gate transistor on a substrate (e.g. claims 21 and 1-14 of Patent No. 6,320,222). Employing the method of the Patent claims for forming the transistor by the claimed method in the present application is apparent and would have been obvious to skill artisan, wherein scope of the claims of the present application is broad enough to encompass the scope of patent claims 1-22 of Patent No. 6,320,222. Forming the transistor on a silicon on insulator (SOI) substrate including an insulating layer on a silicon substrate as taught by Mazure would have been obvious to one of ordinary skill in the art, because these alternative substrates are art recognized alternative for substitution, wherein substrate capacitance is reduced due to the insulating layer formed on the silicon substrate, wherein Mazure teaches (at col 3, lines 1-10) forming a transistor on a substrate, wherein the substrate includes a bulk silicon substrate or a silicon on insulator (SOI) substrate including a silicon layer on an insulating layer on a silicon substrate.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

Response to Amendment

*** Rejection of claim 4 under 35 USC 112, first paragraph, new matter is withdrawn since specification teaches the body region layer 514 having the body region having a thickness of about 0.4 micron.

*** Applicant submitted the statement (at remark pages 29 and 30 filed June 02, 2003) that "...was commonly owned with an application at the time the invention was made...,owned by, or subject to an obligation of assignment to, the same person...". Accordingly, the U.S. Patents 6,150,687 and 6,097,065 are disqualified as prior art through 35 U.S.C. 102(e), (f) or (g) in any rejection under 35 U.S.C. 103(a) in this application.

*** Applicant added co-inventor named Wendell Noble into this application to correct inventorship. The rejection under 35 USC 102(f) using Patent No. 6,320,222 is no longer applicable and withdrawn.

*** The obviousness-type double patenting rejection is maintained since no proper terminal disclaimer is timely submitted.

*** Applicant's other remarks filed June 02, 2003 with respect to claims 1-30 have been considered but are moot in view of the new ground(s) of rejection.

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Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael M. Trinh whose telephone number is (703) 308-2554. The examiner can normally be reached on M-F from 8:30 Am to 4:30 Pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on (703) 308-4905. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

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Michael Trinh
Primary Examiner